LISTING OF THE CLAIMS

1. (Previously presented) A device for exchanging data signals between a first clock domain and a second clock domain, characterized in that the device comprises a serial memory element in which successive data elements are shifted in order from one memory location to a next successive memory location, and a parallel memory element coupled to the serial memory element, the serial memory element comprising at least one memory location more for the data signals than the parallel memory element.

2. (Previously presented) A device as claimed in claim 1, characterized in that the serial memory element is arranged for writing the data signals and the parallel memory element is arranged for reading out the data signals.

3. (Previously presented) A device as claimed in claim 2, characterized in that a first control signal for writing the data signals in the serial memory element can be derived from a first clock signal which is arranged for synchronizing the data signals in the first clock domain, and in that a second control signal for reading the data signals from the parallel memory element can be derived from a second clock signal which is arranged for synchronizing the data signals in the second clock domain.

4. (Previously presented) A device as claimed in claim 1, characterized in that the serial memory element is arranged for reading out the data signals and in that the parallel memory element is arranged for writing the data signals.

5. (Previously presented) A device as claimed in claim 4 characterized in that a third control signal for reading the data signals from the serial memory element can be derived from a first clock signal which is arranged for synchronizing the data signals in the first clock domain, and in that a fourth control signal for writing the data signals in the parallel memory element can be derived from a second clock signal which is arranged for synchronizing data signals in the second clock domain.

6. (Previously presented) A device as claimed in claim 1, characterized in that the device is arranged for adapting a sample rate of the data signals.

7. (Previously presented) A device as claimed in claim 1, characterized in that the device is arranged for changing a modulation scheme of the data signals.

8. (Previously presented) A device as claimed in claim 1, characterized in that the data signals are audio samples.

9. (Previously presented) A module for transferring data signals between a first and a second clock domain, comprising a device as defined in claim 1.

10. (Previously presented) A device for transferring data signals between a first and a second clock domain, comprising a module as claimed in claim 9.